ET-MINI 74165

It is 8BIT Shift Register Parallel-to-Serial Data Conversion that is Parallel-IN, Serial-OUT for SPI Interface. It receives incoming data as parallel type and then sends Output Data as serial type. It supports the maximum Signal Clock at 35MHz.

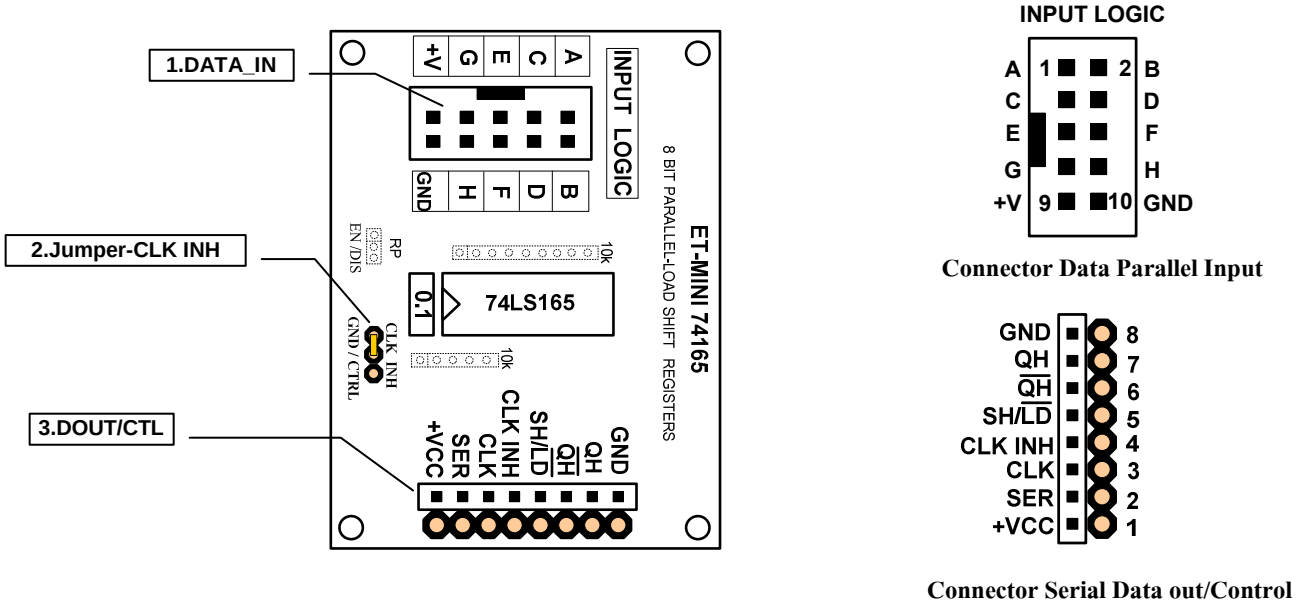


Figure displays the structure of Board ET-MINI 74165 and pin position of Port.

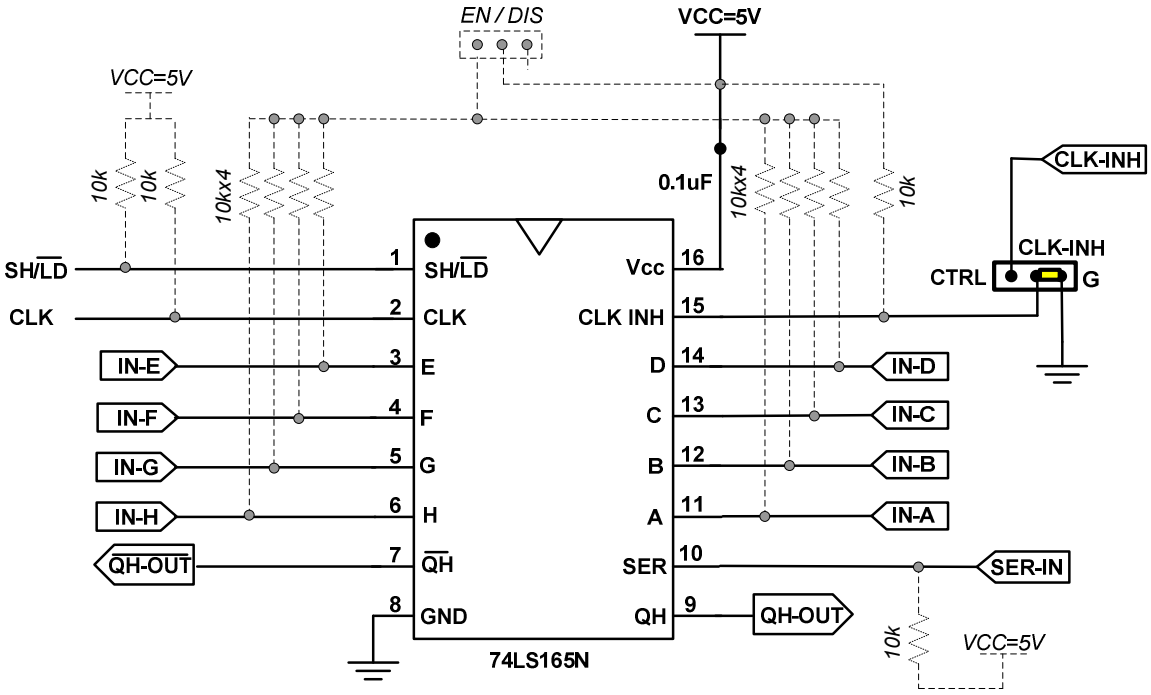
1. **DATA_IN**: It is Connector Parallel Data Input 8Bit(A-H). Connector V+ and GND is Connector 5VDC Power Supply for board that is the same point as +VCC and GND of Connector No.3 DOUT/CTL. It arranges Bit0 of Data Input at the position of PIN A(Pin 1) and Bit7 is arranged at the position of PIN H(Pin 8).
2. **Jumper-CLK INH**: It is Jumper to set and interface Pin CLK INH to Ground or interface with Connector No.3 DOUT/CTL; in this case, user can control signal by self. Normally, it is interfaced with Ground.
3. **DOUT/CTL**: It is Connector that is interfaced to control the operation of Shift Register and receive Data Output at PIN QH serially. Detailed pins are described as follows;
   - ***Pin +VCC,GND***: It is Connector 5VDC Power Supply for board.
   - ***Pin QH, $\overline{QH}$***: It is pin to send Data Output serially and Data Bit7 is the first bit that is sent out first. Data that is sent out from Pin QH is the same Data as the incoming Data Input. On the other hand, Data that is sent out from Pin $\overline{QH}$ is inverted to Data Input or QH.
   - ***Pin SH/$\overline{LD}$***: It is pin to load 8Bit data as parallel type from Input side to Register and this Data is loaded to each

Output of Shift Register. If user wants to load data, this pin must be Logic 0 and it needs to become Logic 1 before shifting data into Pin QH.

- ***Pin CLK INH/CLK***: It is Pin Signal Clock that runs at the Rising Edge Pin(from 0 to 1) to shift a bit data to Pin QH in each time. This Pin Clock has 2 pins. Firstly, it is Pin CLK, it receives Signal Clock to shift data. Secondly, Pin CLK INH; if Pin CLK INH is Logic 1, it stops the operation of Pin CLK; normally, this Pin CLK INH is not used but it always set to be Logic 0.
- ***Pin SER***: It is Pin Serial Data Input that receives Data Output from Pin QH of another Shift Register to expand Input more than 8Bit.

Initial Application

1) Interface 5V Power Supply with board; it needs to choose only one point to interface between Block 10PIN Input Logic or Connector 8PIN.
2) Set Jumper at Pin CLK INH to the GND position.
3) Interface Data Input 8Bit(parallel) that requires sending with Block 10PIN(Input Logic).
4) Start sending Input Data 8Bit and then wait at Pin A-H of Shift Register.
5) Send Signal Logic 0 to Pin SH/$\overline{LD}$ to load all 8Bit Input Data to Shift Register simultaneously. In this case, Data Input Bit 7 is the first bit that is sent out to Pin QH (Data out).
6) Send Signal Logic 1 to Pin SH/$\overline{LD}$ to finish loading the first set of 8Bit Data.
7) When user has already set Pin SH/$\overline{LD}$ to be 1, it reads data from Pin QH and then stores them; in this case, it is Bit 7 of the incoming Data Input.
8) Send Signal Clock at the Rising Edge Pin(from Logic 0 to Logic 1) into Pin CLK to shift Data Input Bit 6 to Pin QH.
9) Read value from Pin QH and then store it again; next, user can send the next Clock to Pin CLK as well. User needs to do these processes until all 8Bit Data are shifted to Pin QH completely. If user wants to send the next data set, please return to Step 4 and repeat the old processes.



**The dotted lines are OPTION that is not added any device.*

Figure displays Circuit of ET-MINI TPIC6B595.